WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of first memory cells for storing either one of first information and second information, arranged at points of intersection between a plurality of word lines and a plurality of first data lines;

a plurality of first dummy cells for storing said first information, arranged at points of intersection between said plurality of word lines and first dummy data lines; and

a plurality of second dummy cells for storing said second information, arranged at points of intersection between said plurality of word lines and second dummy data lines.

2. A semiconductor device according to claim 1, which further comprises:

a first multiplexer connected to one of the ends of said plurality of first data lines;

a second multiplexer connected to one of the ends of said first and second dummy data lines;

a third multiplexer connected to the other end of said plurality of first data lines;

a fourth multiplexer connected to the other ends of said first and second dummy data lines; and

a read circuit connected to said first and second multiplexers; wherein:

when the memory information is written to any of said plurality of first memory cells, said first

multiplexer supplies a second potential smaller than a first potential to one of said plurality of data lines when said third multiplexer supplies said first potential to one of said plurality of first data lines, and supplies said first potential to one of said first data lines when said third multiplexer supplies said second potential to one of said plurality of first data lines.

3. A semiconductor device according to claim 1, which further comprises:

a first multiplexer connected to said plurality of first data lines;

a second multiplexer connected to said first and second dummy data lines;

a read circuit connected to said first and second multiplexers;

a first common data line for connecting said read circuit to said first multiplexer; and

a second common data line for connecting said read circuit to said second multiplexer; wherein:

said read circuit includes a first current mirror circuit connected to said first common data line, a second current mirror circuit connected to said second common data line, a first sense data line connected to said first current mirror circuit, a second sense data line connected to said second current mirror circuit, and a sense amplifier connected to said first and second sense data lines.

4. A semiconductor device according to claim 3, wherein said first current mirror circuit is set so that a current flowing through said first common data line is substantially equal to a current flowing through said first sense data line, and said second current mirror circuit is set so that a current flowing through said first sense data line is substantially 1/2 of a current flowing through said second common data line.

5. A semiconductor device according to claim 4, wherein said plurality of first memory cells and said plurality of first and second dummy cells are so formed as to possess a common construction and store said first or second information by use of a magnetoresistive effect.

6. A semiconductor device according to claim 1, which further comprises:

a plurality of second memory cells for storing said first information or said second information, arranged at the points of intersection between said plurality of word lines and a plurality of data lines;

a first multiplexer connected to said plurality of first data lines;

a second multiplexer connected to said first and second dummy data lines;

a fifth multiplexer connected to said plurality of second data lines; and

a read circuit connected to said first, second and fifth multiplexers; wherein:

said first and second dummy data lines are interposed between said plurality of first data lines and said plurality of second data lines.

7. A semiconductor device according to claim 6, which further comprises:

a first common data line for connecting said read circuit to said first multiplexer;

a second common data line for connecting said read circuit to said second multiplexer; and

a third common data line for connecting said read circuit to a fifth multiplexer; wherein:

said read circuit includes a first current mirror circuit connected to said first common data line, a second current mirror circuit connected to said second common data line, a third current mirror circuit connected to said third common data line, a first sense data line connected to said first current mirror circuit, second and third sense data lines connected to said second current mirror circuit, a fourth sense data line connected to said third current mirror circuit, a first sense amplifier connected to said first and second sense data lines, and a second sense amplifier connected to said third and fourth sense data lines.

8. A semiconductor device according to claim 7, wherein said first current mirror circuit is set so that a current flowing through said first common data

line is substantially equal to a current flowing through said first sense data line, said second current mirror circuit is set so that a current flowing through said second and third sense data lines is substantially equal to 1/2 of a current flowing through said second common data line, and said third current mirror circuit is set so that a current flowing through said third common data line is substantially equal to a current flowing through said fourth sense data line.

9. A semiconductor device according to claim 8, wherein said plurality of first and second memory cells and said plurality of first and second dummy cells are formed into a common construction, and store said first information or said second information by use of a magnetoresistive effect.

10. A semiconductor device according to claim 1, which further comprises:

a plurality of second memory cells for storing said first or second information, arranged at points of intersections between said plurality of word lines and said plurality of second data lines;

a plurality of third dummy cells for storing said first information, arranged at points of intersection between said plurality of word lines and third dummy data lines;

a plurality of fourth dummy cells for storing said second information, arranged at points of intersection between said plurality of word lines and

fourth dummy data lines;

a first multiplexer connected to said plurality of first data lines;

a second multiplexer connected to said first and second dummy data lines;

a fifth multiplexer connected to said plurality of second data lines;

a sixth multiplexer connected to said third and fourth dummy data lines; and

a read circuit connected to said first, second, fifth and sixth multiplexers; wherein:

said first and second multiplexers are connected to said read circuit through a first common data line; and

said fifth and sixth multiplexers are connected to said read circuit through a second common data line.

11. A semiconductor device according to claim 10, wherein said read circuit includes a first current mirror circuit connected to said first common data line, a second current mirror circuit connected to said second common data line, a first sense data line connected to said first current mirror circuit, a second sense data line connected to said second current mirror circuit, and a sense amplifier connected to said first and second sense data line.

12. A semiconductor device according to claim 11, wherein said first current mirror circuit has a first

state in which a current flowing through said first common data line is substantially equal to a current flowing through said first sense data line, and a second state in which a current flowing through said first sense data line is substantially equal to 1/2 of a current flowing through said first common data line, said second current mirror circuit has a third state in which a current flowing through said second common data line is substantially equal to a current flowing through said second sense data line, and a fourth state in which a current flowing through said second data line is substantially equal to 1/2 of a current flowing through said second data line, said first current mirror circuit operates in said first state and said second current mirror circuit operates in said fourth state when memory information is read out from said plurality of first memory cells, and said first current mirror circuit operates in said second state and said second current mirror circuit operates in said third state when the memory information is read out from said plurality of second memory cells.

13. A semiconductor device according to claim 12, wherein said plurality of first and second memory cells and said plurality of first, second, third and fourth dummy cells are formed into a common construction, and store said first information or said second information by use of a magnetoresistive effect.

14. A semiconductor device according to claim 10,

which further comprises:

a plurality of first redundancy memory cells arranged at points of intersection between said plurality of word lines and a first redundancy data line;

a plurality of second redundancy memory cells arranged at points of intersection between said plurality of word lines and a second redundancy data line;

a first redundancy multiplexer connected to said first redundancy data line; and

a second redundancy multiplexer connected to said second redundancy data line; wherein:

said first redundancy multiplexer is connected to said first common data line;

said second redundancy multiplexer is connected to said second common data line;

when any defect of said plurality of first memory cells, said plurality of first dummy cells or said plurality of dummy cells exists, said first redundancy data line replaces said plurality of first data lines, said plurality of first dummy data lines or said plurality of second dummy data lines having said defect; and

when any defect of said plurality of second memory cells, said plurality of third dummy cells or said plurality of fourth dummy cells exists, said second redundancy data line replaces said plurality of

second data lines, said plurality of dummy data lines or said plurality of fourth dummy data lines having said defect.

15. A semiconductor device according to claim 14, which further comprises:

a normal column address decoder for controlling the operation state of said first, second, fifth and sixth multiplexers; and

a redundancy column address decoder for controlling the operation state of said first and second redundancy multiplexers; wherein:

said normal column address decoder includes a normal column address signal driver for outputting a column address signal for controlling the operation state of said first and fifth multiplexers and a dummy column address signal driver for outputting a column address signal for controlling the operation state of said second and sixth multiplexers, and a redundancy column address detection circuit for selecting and activating said normal column address signal driver or said dummy column address signal driver and said redundancy column address signal driver.

16. A semiconductor device according to claim 15, wherein said redundancy column address detection circuit includes a redundancy column address memory circuit for storing the information of said defect.

17. A semiconductor device according to claim 16, wherein said plurality of first and second memory

cells, said plurality of first, second, third and fourth dummy cells and said plurality of first and second redundancy memory cells are formed into a common construction, and store said first information or said second information by use of a magnetoresistive effect.

18. A semiconductor device comprising:

a plurality of first memory cells arranged at points of intersection between a plurality of word lines and a plurality of first data lines;

a plurality of second memory cells arranged at points of intersection between said plurality of word lines and a plurality of second data lines;

a plurality of first dummy cells arranged at points of intersection between said plurality of word lines and first dummy data lines;

a plurality of second dummy cells arranged at points of intersection between said plurality of word lines and second dummy data lines;

a plurality of third memory cells arranged at points of intersection between said plurality of word lines and a plurality of third data lines;

a plurality of fourth memory cells arranged at points of intersection between said plurality of word lines and a plurality of fourth data lines;

a plurality of third dummy cells arranged at points of intersection between said plurality of word lines and a plurality of third dummy data lines;

a plurality of fourth dummy cells arranged at

points of intersection between said plurality of word lines and a plurality of fourth dummy data lines;

a first multiplexer connected to said plurality of first and second data lines;

a second multiplexer connected to said first and second dummy data lines;

a third multiplexer connected to said plurality of third and fourth data lines;

a first common data line to which said plurality of first data lines are connected through said first multiplexer;

a second common data line to which said plurality of second data lines are connected through said first multiplexer;

a third common data line to which said plurality of third data lines are connected through said third multiplexer;

a fourth common data line to which said plurality of fourth data lines are connected through said fourth multiplexer;

a first switch connected between said first and third common data lines;

a second switch connected between said second and fourth common data lines;

a first read circuit connected between said first and second common data lines; and

a second read circuit connected between said third and fourth common data lines; wherein:

memory information mutually complementary are written to said plurality of first dummy cells and said plurality of second dummy cells;

memory information mutually complementary are written to said plurality of third dummy cells and said plurality of fourth dummy cells;

said first dummy data line is connected to said first common data line through said second multiplexer;

said second dummy data line is connected to said third common data line through said second multiplexer;

said third dummy data line is connected to said second common data line through said fourth multiplexer; and

said fourth dummy data line is connected to said fourth common data line through said fourth multiplexer.

19. A semiconductor device according to claim 18, wherein said first switch is turned on when the memory information is read out from any of said plurality of second or fourth memory cells, and said second switch is turned on when the memory information is read out from any of said plurality of first or third memory cells.

20. A semiconductor device according to claim 19, wherein said first read circuit includes a first current mirror circuit connected to said first common

data line, a second current mirror circuit connected to said second common data line, a first sense data line connected to said first current mirror circuit, a second sense data line connected to said second current mirror circuit and a first sense amplifier connected to said first and second sense data lines, and said second read circuit includes a third current mirror circuit connected to said third common data, a fourth current mirror circuit connected to said fourth common data line, a third sense data line connected to said third current mirror circuit, a fourth sense data line connected to said fourth current mirror circuit and a second sense amplifier connected to said third and fourth sense data lines.

21. A semiconductor device according to claim 20, wherein said first to fourth current mirror circuits are set so that a current flowing through the corresponding first to fourth common data lines is substantially equal to a current flowing through the corresponding first to fourth sense data lines.

22. A semiconductor device according to claim 21, wherein said plurality of first, second, third and fourth memory cells and said plurality of first, second, third and fourth dummy cells are formed into a common construction, and store said first information or said second information by use of a magnetoresistive effect.

23. A semiconductor device according to claim 1,

wherein said plurality of first memory cells and said plurality of first and second dummy cells each include a transistor and an MTJ (magnetic tunnel junction) device connected in series with said transistor.